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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WANG, ALBERT C	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,173	LEE, TERRY R..	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-45,48-86 and 88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *83-86 and 88* is/are allowed.

6)☒ Claim(s) *1-5,7-45 and 48-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *November 15, 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed June 14, 2004.

2. Claims 1-5, 7-45, 48-86, and 88 are pending. Applicants have incorporated canceled claims 6 and 47 into respective independent claims 1 and 42. Applicants have also amended all independent claims (1, 42, 68, 83, 84, and 88) to include the limitation that the data read clock and data write clock are independent signals. Claims 4, 5, 7, 8, 13, 44, and 45 were amended in response to rejection under 35 U.S.C 112 second paragraph. Claims 9, 21, 48, and 51 are also amended

3. Applicant's arguments with respect to claims 1-5, 7-45, 48-86, and 88 have been considered but are moot in view of the new ground(s) of rejection.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objections

5. Claim 42 objected to because of the following informalities: the punctuation of claim 42 is inconsistent with that of claims 68 and 83 in that: on line 2 after "comprising" there is a colon; on line 3 after "paths" there is semi-colon instead of a comma; and on lines 5 after "bus" there is a semi-colon instead of ", and". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. Claims 1-3, 7-11, 21-24, 33 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Perino et al., U.S. Patent No. 6,426,984 ("Perino").

As per claim 1, Perino discloses a method of providing clocking signals over a bus, said method comprising:

providing a first clock signal which travels over a first conductive path of said bus in a first direction (Fig. 5, clock2 over paths 30 and 34);

providing a second clock signal which travels over a second conductive path of said bus in a second direction opposite to said first direction (Fig. 5, clock1 over paths 28 and 32); and

causing said first and second clock signals to have a predetermined phase relationship with respect to each other at a predetermined location on said bus (Fig. 5, circuit 74 adjusts clock latency at nodes A and B).

wherein said first and second clock signals are independent clocks signals (Figs. 5 & 6; Col. 6, lines 15-31, eliminates the turnaround path 29 of fig. 1 and creates a new clock signal), one of said first and second clock signals is a data write clock signal, and the other of said first and second clocks signals is a data read clock signal.

In Perino, clock1 is for reading data from a slave device; and clock2 is writing data to a slave device. The functions of clock1 and clock2 can be more clearly understood by examining the prior art in Fig. 1, of which the system of Fig. 5 is an improvement (Col. 5, lines 42-60). In Fig. 1, "the transmission of data from the master device 24 to the slave devices 26 is timed by the clock signals on the clock-from-master path 30" and "transmission of the data from the slave devices 26 to the master device 24 is timed by the clock signals of the clock-to-master path 28" (Col. 1, line 60 – Col. 2, line 4). Thus, the clock1 and clock2 signals in Fig. 5 correspond to data read and data write clock signals.

As per claim 2, Perino discloses said predetermined phase relationship is substantially an in-phase relationship (Col. 6, lines 32-38).

As per claim 3, Perino discloses said detecting the phase relationship of said first and second clock signals at said predetermined location and adjusting at least one of said first and second clock signals (Fig. 5 & 6).

As per claims 7 and 8, Perino discloses said predetermined location may be relocated along the length of said first and second conductive paths (Figs. 5 and 7, location at A&B is changed to A'&B').

As per claim 9, Perino discloses each of said input/output devices comprise a memory subsystem (Claim 20).

As per claims 10 and 11, Perino discloses the phase deviations of said data write and data read clock signals (Col. 5, lines 50-60).

As per claim 21, Perino discloses at least one memory subsystem (Claim 20) and obtaining said predetermined phase relationship at said predetermined location (Col. 6, lines 32-38).

As per claim 22, Perino discloses said data write signal path is terminated (Fig. 5, termination block 31)

As per claims 23 and 24, Perino discloses said data read clock signal path is a loop back signal path (path 28).

As per claim 33 and 34, Perino discloses minimizing the phase between the data read clock and data write clock signals (Col. 5, lines 50-60).

Claim Rejections - 35 USC § 103

7. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claims 1 and 2 above, in further view of Co et al., U.S. Patent No. 6,584,576.

As per claims 4 and 5, Perino does not expressly teach configuring the signal propagation characteristics of at least one of said first and second conductive paths to obtain said predetermined relationship. Co teaches using adjusting clock timing relative to another line (Fig. 3, using delay elements 12 and 16 on clock to master line; Fig. 4, using delay 24 on clock to master line; Cols. 3 and 4). A predetermined phase relationship between signals at a predetermined location a bus (Figs. 3, location at module 10; Fig. 4, location at module 10-1; Col. 3, lines 28-35, minimize timing skew at module 10) is obtained by configuring signal propagation characteristics (Col. 3, lines 46-61, positive or negative delay corresponds to making traces longer or shorter; Col. 4, lines 50-58).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Co's configuring signal propagation characteristics to Perino's method. Configuring signal propagation characteristics or using an alternative method to obtain a phase relationship between two signal lines is a matter of design.

8. Claims 12-14 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claim 9 above, in further view of Yamagishi et al., U.S. Patent No. 6,366,190 ("Yamagishi").

As per claims 12-14 and 29, Perino does not expressly teach details of the memory subsystem to include a date write clock regeneration circuit. Yamagishi teaches a data write clock regeneration circuit for providing a plurality of regenerated data write clock signals to memory storage devices (Fig. 1, clock generator 4 and storage elements 5a-n). At the time of the invention, it would have been obvious to one of ordinary skill in

to apply Yamagishi's data write clock regeneration to Perino's method. A motivation for doing so would have been to ensure the integrity of the system by compensating for loading of the clock signal.

9. Claims 15-20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claim 9 above, in further view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claims 15-20, Perino does not expressly teach details of the method to include a data read clock regeneration circuit. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Perino's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Perino/Magro further teaches a plurality of additional read clock signal paths.

10. Claims 30-32, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Yamagishi, as applied to claim 29 above, in further view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claims 30-32 and 35, Perino/Yamagishi does not expressly teach issuing a plurality of data read clock signals from said memory controller. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to

apply Magro's clock regeneration circuit to Perino's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Perino/Magro further teaches a plurality of additional read clock signals.

As per claim 36, Yamagishi teaches registers for receiving data in general at the memory subsystem (Fig. 4, group 22). Magro teaches command and address data paths, separate from the read/write data paths, that lead to the memory subsystem (Fig. 2b). Thus it would have been obvious to a have a register for command and address data.

11. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Yamagishi/Magro, as applied to claim 36 above, in further view of Mizukami et al., U.S. Patent No. 5,422,858 ("Mizukami").

As per claim 37, Perino/Yamagishi/Magro does not expressly teach the data write signal provided to said register is at a lower frequency than the data write clock signals provided to said memory devices. Mizukami teaches multiplying clock signals provided to said memory devices (Fig. 3, multiplied clock provided to ram core). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Mizukami's clock multiplying to Perino/Yamagishi/Magro's method. A motivation for doing would have been to optimize clock timing within the memory devices (Yamagishi, Col. 1, line 58 – Col. 2, line 5).

12. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claim 9 above, in further view of Gillingham et al., U.S. Patent No. 6,510,503 ("Gillingham").

As per claim 38, Perino does not expressly teach a memory module capable of being connected to said bus. Gillingham teaches such a memory module (Figs. 14a &b). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gillingham's socket to Perino's method. A motivation for doing so would have been to facilitate replacement by modularizing components.

As per claim 39-41, Gillingham teaches each memory subsystem comprises a plurality of memory storage devices (Figs. 13 and 14).

13. Claims 25-28, 42, 43, 46, 48-51, 68, 72, 73, 78-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino, as applied to claims 1, 3, 6, and 21 above, in further view Gasbarro et al., U.S. Patent No. 5,432,823 ("Gasbarro").

As per claim 42, Perino teaches a clock system for a data bus, comprising:

a data bus comprising:

a plurality of data paths (Fig. 1, slash on data bus 36 indicates plurality of paths; Col. 1, lines 14-18, 48-59);

a first clock signal path for propagating a first clock signal in a first direction along said bus (Fig. 5, paths 30 and 34 for clock2);

a second clock signal path for propagating a second clock signal in a second direction opposite to said first direction along said bus (Fig. 5, paths 28 and 32 for clock1);

a bus controller for issuing said first clock signal in said first clock signal path (Fig. 5, master 24 issues clock2); and

circuitry for causing said first and second clock signals to have a predetermined phase relationship with respect to each other at a predetermined location along said bus (Fig. 5, clock latency adjustment circuit 74);

wherein said first and second clock signals are independent signals (Figs. 5 & 6; Col. 6, lines 15-31, eliminates the turnaround path 29 of fig. 1 and creates a new clock signal), one of said first and clock signals is a data write clock signal, the other of said first and second clock signals is a data read clock signal (Col. 5, lines 42-60, fig. 5 is an improvement upon system of fig. 1; Col. 1, line 60 – Col. 2, line 4, "the transmission of data from the master device 24 to the slave devices 26 is timed by the clock signals on the clock-from-master path 30" and "transmission of the data from the slave devices 26 to the master device 24 is timed by the clock signals of the clock-to-master path 28").

Perino does not expressly teach issuing said second clock signal from said bus controller. Perino does teach changing the location of the circuitry (Figs. 5 & 8, circuit 74 is moved from clock generator 72 to master 24). Gasbarro teaches a bus controller that issues both clock signals (Fig. 2, master device). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gasbarro's issuing said first clock signal from the bus controller to Perino's clock system, since Gasbarro is incorporated by reference (Col. 1, lines 14-18).

As per claim 43, Perino teaches said predetermined phase relationship is substantially an in-phase relationship (Col. 6, lines 32-38).

As per claim 46, Perino teaches said circuitry is is a phase detecting circuit associated with said bus controller (Figs. 6 & 8).

As per claim 48, Perino teaches a plurality of input/output devices coupled to said bus (Fig. 5, slaves 26A-N).

As per claims 49 and 50, Perino teaches said predetermined location may be relocated along the length of said first and second conductive paths (Figs. 5 and 7, location at A&B is changed to A'&B').

As per claim 51, Perino teaches each of said input/output devices comprise a memory subsystem (Claim 20).

As per claim 25, Gasbarro teaches terminating said loop back signal path at said memory controller (Fig. 2, RLCK0 and RCLK1).

As per claim 26, since the bus controller issues both data write clock and data read clock signals, it would have been obvious to derive both clocks from the same clock source in order to avoid the complexity of an additional clock generator.

As per claim 27, Perino teaches using a phase lock loop (Col. 6, lines 32-38).

As per claim 28, Perino teaches adjusting the relative phase relationship (Col. 6, lines 1-14).

As per claim 68, Perino teaches a memory system comprising:

a data bus comprising

a plurality of read/write data paths (Fig. 1, slash on data bus 36 indicates plurality of paths; Col. 1, lines 14-18, 48-59),

a data write clock signal path for propagating a data write clock signal in a first direction along said bus (Fig. 5, paths 30 and 34 for clock2; Col. 5, lines 42-60, fig. 5 is an improvement upon system of fig. 1; Col. 1, line 60 – Col. 2, line 4, "the transmission of data from the master device 24 to the slave devices 26 is timed by the clock signals on the clock-from-master path 30"), and

a data read clock signal path for propagating a data read clock signal in a second direction opposite to said first direction along said bus (Fig. 5, paths 28 and 32 for clock1; Col. 5, lines 42-60, fig. 5 is an improvement upon system of fig. 1; Col. 1, line 60 – Col. 2, line 4, "transmission of the data from the slave devices 26 to the master device 24 is timed by the clock signals of the clock-to-master path 28");

a memory controller coupled to said bus for issuing said date write clock signal on said data write clock signal path (Fig. 5, master 24 issues clock2; Claim 21) and for setting a predetermined phase relationship between said data write and data read clock signals at a predetermined phase relationship between said data write and data read clock signals at a predetermined location along said bus (Fig. 8, clock latency adjustment circuit 74 located in master 24); and

at least one memory subsystem coupled to said bus for exchanging data with said memory controller in accordance with timing set by said data write and data read clock signals (Fig. 5, slaves 26A-N; Claim 20);

wherein said data write clock signal and said data read clock signal are independent signals (Figs. 5 & 6; Col. 6, lines 15-31, eliminates the turnaround path 29 of fig. 1 and creates a new clock signal).

Perino does not expressly teach issuing said read clock signal from said memory controller. Perino does teach changing the location of the circuitry (Figs. 5 & 8, circuit 74 is moved from clock generator 72 to master 24). Gasbarro teaches a bus controller that issues both clock signals (Fig. 2, master device). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gasbarro's issuing both clock signals from the bus controller to Perino's memory system, since Gasbarro is incorporated by reference (Col. 1, lines 14-18).

As per claim 72, Perino teaches an associated phase lock loop for maintaining said predetermined phase relationship (Fig. 6).

As per claim 78, Perino teaches said data write signal path is terminated (Fig. 5, termination block 31), and said data read clock signal path is a loop back signal path (path 28).

As per claims 79 and 80, Gasbarro teaches terminating said loop back signal path at said memory controller (Fig. 2, RLCK0 and RCLK1).

As per claims 73, 81 and 82, Perino teaches a plurality of memory subsystems (Fig. 5, slaves 26A-N) and minimizing clock latency (Col. 5, lines 50-60).

14. Claims 44 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro, as applied to claim 42 above, in further view of Co et al., U.S. Patent No. 6,584,576.

As per claims 44 and 45, Perino does not expressly teach configuring the signal propagation characteristics of at least one of said first and second conductive paths to obtain said predetermined relationship. Co teaches using adjusting clock timing relative

to another line (Fig. 3, using delay elements 12 and 16 on clock to master line; Fig. 4, using delay 24 on clock to master line; Cols. 3 and 4). A predetermined phase relationship between signals at a predetermined location a bus (Figs. 3, location at module 10; Fig. 4, location at module 10-1; Col. 3, lines 28-35, minimize timing skew at module 10) is obtained by configuring signal propagation characteristics (Col. 3, lines 46-61, positive or negative delay corresponds to making traces longer or shorter; Col. 4, lines 50-58).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Co's configuring signal propagation characteristics to Perino/Gasbarro's method. Configuring signal propagation characteristics or using an alternative method to obtain a phase relationship between two signal lines is a matter of design.

15. Claims 69-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro, as applied to claim 68 above, further in view of Gillingham et al., U.S. Patent No. 6,510,503 ("Gillingham").

As per claim 69, Perino/Gasbarro does not expressly teach the details of each memory subsystem. Gillingham teaches a memory subsystem comprising a plurality of memory devices (Fig. 14a, memory devices 196). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Gillingham's plurality of memory devices to Perino/Gasbarro's memory subsystem. A motivation for doing so would have been to ensure the integrity of Perino/Gasbarro's memory subsystem.

As per claims 70 and 71, Perino discloses said predetermined location may be relocated along the length of said first and second conductive paths (Figs. 5 and 7, location at A&B is changed to A'&B').

16. Claims 52-67 and 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro/Gillingham, as applied to claim 69 above, further in view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claim 75, Perino/Gasbarro/Gillingham, as applied to claim 69, does not expressly teach details of the memory system to include a data read clock regeneration circuit. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Perino/Gasbarro/Gillingham's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Gasbarro/Magro further teaches a plurality of additional read clock signal paths.

As per claim 76, Gillingham teaches a motherboard (Fig. 13a).

As per claim 77, Gasbarro teaches a transmitting device which generates data write clock and read clock signals (Fig. 3, element 132).

As per claims 52-67, since Perino/Gasbarro/Gillingham/Magro teaches the memory system of claims 68-73 and 75-82, the combination teaches the claimed clock system.

As per claims 70 and 71, Perino discloses said predetermined location may be relocated along the length of said first and second conductive paths (Figs. 5 and 7, location at A&B is changed to A'&B').

16. Claims 52-67 and 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro/Gillingham, as applied to claim 69 above, further in view of Magro et al., U.S. Patent No. 6,516,362 ("Magro").

As per claim 75, Perino/Gasbarro/Gillingham, as applied to claim 69, does not expressly teach details of the memory system to include a data read clock regeneration circuit. Magro teaches a coupling a clock regeneration circuit coupled to a clock signal path (Fig. 2b, clock driver 116). At the time of the invention, it would have been obvious to one skilled in the art to apply Magro's clock regeneration circuit to Perino/Gasbarro/Gillingham's read clock signal path. A motivation for doing so would have been to compensate for loading of the clock signal (Magro, Col. 11, lines 5-10). Since Magro teaches a plurality of signal paths (Fig. 2b, output from clock driver 116), Gasbarro/Magro further teaches a plurality of additional read clock signal paths.

As per claim 76, Gillingham teaches a motherboard (Fig. 13a).

As per claim 77, Gasbarro teaches a transmitting device which generates data write clock and read clock signals (Fig. 3, element 132).

As per claims 52-67, since Perino/Gasbarro/Gillingham/Magro teaches the memory system of claims 68-73 and 75-82, the combination teaches the claimed clock system.

17. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perino/Gasbarro, as applied to claim 68 above, in further view of Yamagishi et al., U.S. Patent No. 6,366,190 ("Yamagishi").

As per claim 74, Perino/Gasbarro, as applied to claim 68, does not expressly teach details of the memory subsystem to include a date write clock regeneration circuit. Yamagishi teaches a data write clock regeneration circuit for providing a plurality of regenerated data write clock signals to memory storage devices (Fig. 1, clock generator 4 and storage elements 5a-n). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Yamagishi's data write clock regeneration to Perino/Gasbarro's memory subsystem. A motivation for doing so would have been to ensure the integrity of the system by compensating for loading of the clock signal.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 703-305-5385. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
August 10, 2004

THOMAS LEE
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TECHNOLOGY CENTER 2100